

Fig. 3 A layer of dielectric is deposited followed by a lithography Patterning to open the area where MIMCap need to be built.

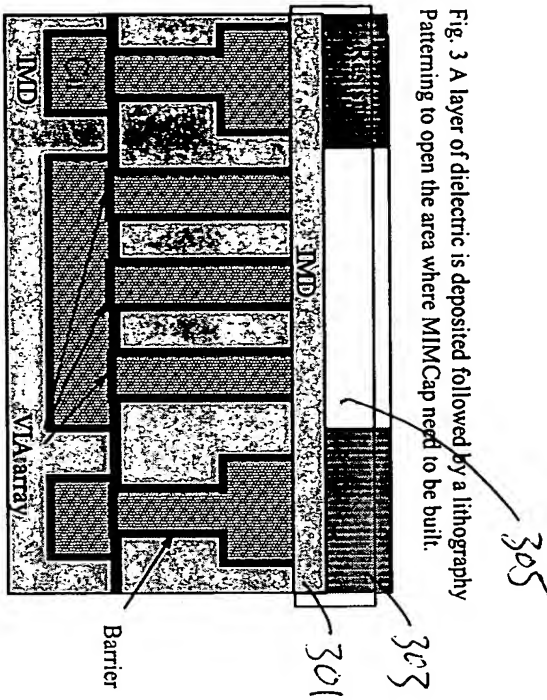


Fig. 4 To selectively etch dielectric and strip the residual resist This process leaves Cu VIAs stand alone

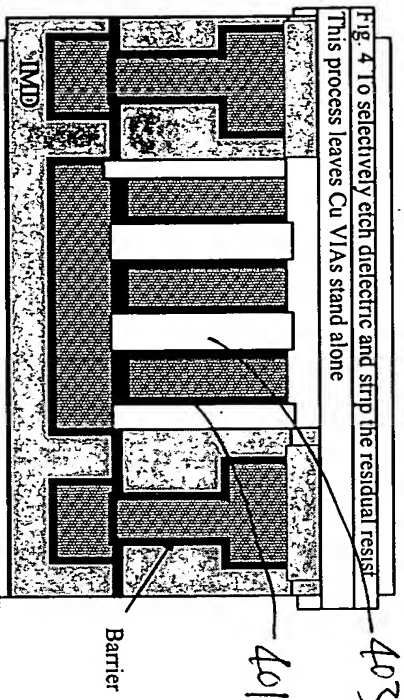
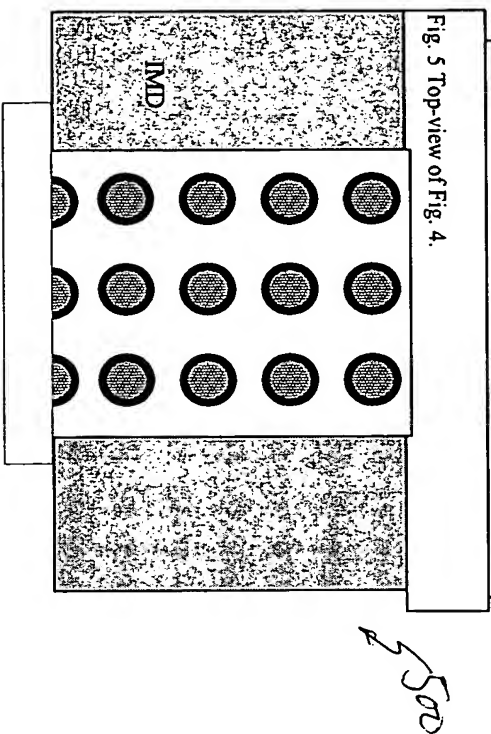


Fig. 5 Top-view of Fig. 4.



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